Claims

What is claimed is:

1. A signal processing system for delay locked loop processing, comprising:

an interpolator for generating time shifted samples based on input samples;

first and second correlators, coupled to the time shifted samples and the input samples, for extracting, respectively, ontime control symbol samples and data symbol samples;

a third correlator, coupled to the time shifted samples and the input samples, for extracting first non-ontime control symbol samples; and

wherein the first non-ontime control symbol samples and the ontime control symbol samples are used for extracting second non-ontime symbol samples.

2. The signal processing system of claim 1, further comprising a postcorrelator interpolator for extracting the second non-ontime symbol samples using the first non-ontime control symbol samples and the ontime control symbol samples.

3. The signal processing system of claim 2, wherein the postcorrelator interpolator is implemented in an ASIC.

4. The signal processing system of claim 2, wherein the postcorrelator interpolator comprises a software implemented interpolator.

5. The signal processing system of claim 1, wherein the interpolator generates time shifted chip samples based on input CDMA chip samples and the system further comprises:

a first multiplexer for outputting an ontime correlator signal from the input CDMA chip samples and the time shifted chip samples generated by the interpolator for input into both the first and second correlators;

a second multiplexer for outputting a non-ontime correlator signal from the input CDMA chip samples and the time shifted chip samples generated by the interpolator for input into the third correlator; and

wherein the first multiplexer enables ontime input CDMA chip samples to be input into the first and second correlators, and the second multiplexer enables non-ontime chip samples to be input into the third correlator.

6. The signal processing system of claim 1, wherein the first non-ontime control symbol samples comprise early symbol samples, and the second non-ontime symbol samples comprise late symbol samples.

7. The signal processing system of claim 1, wherein the first non-ontime control symbol samples comprise late symbol samples, and the second non-ontime symbol samples comprise early symbol samples.

8. A CDMA receiver, comprising:

an analog processing circuit for removing a carrier frequency from a received CDMA signal and for sampling the received CDMA signal at a predetermined sampling rate to produce corresponding CDMA chip samples;

an interpolator for receiving the CDMA chip samples from the analog processing circuit and for generating time shifted chip samples from the CDMA chip samples;

first and second correlators for extracting, respectively, ontime control symbol samples and data symbol samples from one of the CDMA chip samples and the time shifted chip samples;

a third correlator for extracting first non-ontime control symbol samples from one of the CDMA chip samples and the time shifted chip samples; and

wherein the first non-ontime control symbol samples and the ontime control symbol samples are used for extracting second non-ontime symbol samples for delay locked loop processing.

9. The CDMA receiver of claim 8, further comprising a postcorrelator interpolator for extracting the second non-ontime symbol samples using the first non-ontime control symbol samples and the ontime control symbol samples.

10. The CDMA receiver of claim 9, wherein:

the first and second correlators are for extracting, respectively, the ontime control symbol samples and data symbol samples at a chip sampling rate;

the third correlator is for extracting the first non-ontime control symbol samples at the chip sampling rate; and

the postcorrelator interpolator is for extracting the second non-ontime symbol samples at a symbol sampling rate.

11. The CDMA receiver of claim 9, wherein the postcorrelator interpolator is implemented in an ASIC.

12. The CDMA receiver of claim 9, wherein the postcorrelator interpolator comprises software implemented interpolator.

13. The CDMA receiver of claim 8, further comprising:

a first multiplexer for outputting an ontime correlator signal from the CDMA chip samples and the time shifted chip samples for input into both the first and second correlators; and

a second multiplexer for outputting a non-ontime correlator signal from the CDMA chip samples and the time shifted chip samples for input into the third correlator.

14. The CDMA receiver of claim 8, wherein the first non-ontime control symbol samples comprise early symbol samples, and the second non-ontime symbol samples comprise late symbol samples.

15. The CDMA receiver of claim 8, wherein the first non-ontime control symbol samples comprises late symbol samples, and the second non-ontime symbol samples comprise early symbol samples.

16. The CDMA receiver of claim 8, wherein the analog processing circuit is for sampling the received CDMA signal at a sampling rate that is at least twice a chip rate to produce corresponding CDMA chip samples.

17. A method of processing samples for delay locked loop processing, comprising:

interpolating between received samples to generate time shifted samples;

extracting ontime control symbol samples from one of the received samples and the time shifted samples;

extracting first non-ontime control symbol samples from one of the received samples and the time shifted samples; and

subsequently extracting second non-ontime symbol samples based on the first non-ontime control symbol samples and the ontime control symbol samples.

18. The method of claim 17, wherein the subsequently extracting second non-ontime symbol samples based on the first non-ontime control symbol samples and the ontime control symbol samples comprises subsequently interpolating, at a symbol rate, the first non-ontime control symbol samples and the control symbol samples to provide the second non-ontime symbol samples.

19. The method of claim 17 wherein the received samples are CDMA chip samples and the time shifted samples are time shifted chip samples.